Registration No.: | | | | | | | | | | |

Total Number of Pages: 02 **Course: B.Tech/IDD (B.Tech and M.Tech)**
Sub_Code: CSPC2005

4th Semester Regular Examination: 2024-25
SUBJECT: Computer Organization and Architecture
BRANCH(S): CE, CSE, CSEAI, CSEAIML, CSEDS, CSIT, CST, IT
Time: 3 Hours
Max Marks: 100
Q.Code: S498
Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Represent (510) in binary signed magnitude and unsigned magnitude.
b) Evaluate $(-55)_{10} + (-54)_{10}$ and represent the result in binary.
c) Specify the location where the overflow bit is stored in an addition circuit.
d) State whether the control bus is unidirectional or bidirectional, and justify.
e) Explain how size and speed vary across different levels of memory hierarchy.
f) Describe the function of the instruction MOV A, M.
g) List the input signals required by a memory unit.
h) Define a block in the context of cache memory.
i) List the basic components of a microprocessor.
j) State the primary purpose of interrupts in a computer system.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Differentiate between RISC and CISC architectures.
b) Explain different types of data transfer in DMA.
c) Define addressing mode. Explain five types with suitable examples.
d) Represent a space-time diagram for the execution of 12 instructions using a 4-stage pipeline.
e) Distinguish between a hardwired control unit and a microprogrammed control unit.
f) Explain the concept of cache coherence in multiprocessor systems.
g) Design adder and subtractor circuits using suitable registers.
h) Explain the concept of memory interleaving with suitable examples.
i) Draw a 4 × 6 memory structure showing address, data, and control buses.
j) Describe the basic components of a computer system based on the Von Neumann architecture.

k) Store the below 8085 instruction in a memory from 2400H onwards by showing its memory locations:
LXI H, 2300H
MVI A, 15H
MVI B, 16H
ADD B
HLT

l) Explain Flynn's classification of computer architectures.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four) **(16 x 2)**

Q3 Demonstrate Booth's multiplication algorithm with a flowchart. Perform the multiplication of (+13) × (–11). **(16)**

Q4 Explain different types of circuitries in a I/O subsystem. Show the flow of information with a suitable diagram. **(16)**

Q5 Describe the instruction execution cycle using a state diagram. Apply the process to execute LXI H, 2300H **(16)**

Q6 Discuss the concept of virtual memory. Compute page faults using FIFO, LRU, and Optimal algorithms for the reference string 1 2 3 4 1 2 5 1 2 3 4 5 with 3 and 4 frames. **(16)**